Avalon bus ST interface

Both ST data source and ST data sink interfaces support a ready latency of zero.

You can use Avalon Streaming (Avalon-ST) interfaces for components that drive high bandwidth, low latency, unidirectional data. Typical applications include multiplexed streams, packets, and DSP data.

Consult the Arria 10 Avalon-ST Interface with SR-IOV PCIe Solutions User Guide for features of this IP core.

The Avalon Memory-Mapped (Avalon-MM) interface specification is designed to accommodate peripheral development for the system-on-a-programmable-chip (SOPC) environment.

Avalon Tri-State Conduit Interface (Avalon-TC) --an interface to support connections to off-chip peripherals. Multiple peripherals can share pins through signal multiplexing, reducing the pin count of ...

The Hard IP for PCI Express using the Avalon Streaming (Avalon-ST) interface is the most flexible variant. However, this variant requires a thorough understanding of the PCIe® Protocol. The ...

The Avalon interface family defines interfaces appropriate for streaming high-speed data, reading and writing registers and memory, and controlling off-chip devices.

Avalon interfaces Avalon interfaces are an open standard (no licens or royalty required to develop and sell products that use, or are based on Avalon Interfaces)

For example, the Avalon-MM interface includes optional beginbursttransfer and burstcount signal types used only for components that support bursting. The Avalon-ST interface includes the optional ...

When discussing Avalon bus transfers, it is important to pay attention to which side of the bus is the focus: the master port interface or the slave port interface.

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